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Ambient condition bias stress stability of vanadium (IV) oxide phthalocyanine based p-channel organic field-effect transistors

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Abstract

High bias-stress stability and low threshold voltage (V_{th}) shift under ambient conditions are highly desirable for practical applications of organic field-effect transistors (OFETs). We demonstrate here a 20-fold enhancement in the bias-stress stability for hexamethyldisilazane (HMDS) treated vanadium (IV) oxide phthalocyanine (VOPc) based OFETs as compared to the bare VOPc case under ambient conditions. VOPc based OFETs were fabricated on bare (non treated) SiO_2 and a HMDS monolayer passivated SiO_2 layer, with an operating voltage of 40 V. The devices with top contact gold (Au) electrodes exhibit excellent p-channel behavior with a moderate hole mobility for the HMDS-treated device. It is demonstrated that the time dependent ON-current decay and V_{th} shift can be effectively controlled by using self-assembled monolayers of HMDS on the VOPc layer. For the HMDS-treated case, the bias stress stability study shows the stretched exponential decay of drain current by only ~15% during the long-term operation with constant bias voltage under ambient conditions, while it shows a large decay of >70% for the nontreated devices operated for 1000 s. The corresponding characteristic decay time constant (τ) is 10^4 s for the HMDS treated case, while that of the the non-treated SiO_2 case is only ~480 s under ambient conditions. The inferior performance of the device with bare SiO_2 is traced to the charge trapping at the voids in the inter-grain region of the films, while it is almost negligible for the HMDS-treated case, as confirmed from the AFM and XRD analyses. It is believed that HMDS treatment provides an excellent interface with a low density of traps and passivates the dangling bonds, which improve the charge transport characteristics. Also, the surface morphology of the VOPc film clearly influences the device performance. Thus, the HMDS treatment provides a very attractive approach for attaining long-term air stability and a low V_{th} shift for the VOPc based OFET devices.

Keywords: bias stress stability, organic field effect transistor, HMDS monolayer, stretched exponential decay

 Supplementary material for this article is available [online](#)

(Some figures may appear in colour only in the online journal)

1. Introduction

Organic field-effect transistors (OFETs) are the fundamental building blocks of low cost integrated circuits, such as active matrix displays [1, 2], chemical or biological sensors [3, 4], and radio-frequency identification (RFID) tags [5] etc.

Furthermore, high performance OFETs are essential for various optoelectronic applications, such as organic light emitting diodes (OLEDs) and organic light emitting field-effect transistors (OLFETs) [6]. The bulk and interface properties of the dielectrics play a critical role in the electrical performance of the final device, since charge carriers are restricted

to the first few nanometers from the dielectric interface [7, 8]. Engineering the surface chemistry of the dielectric is a key parameter to tune the electrical performance of organic semiconductor based OFETs. It has been shown that the passivation by self-assembled monolayers (SAMs) of alkyl-silanes on the inorganic oxide dielectric (specifically on SiO₂) can increase the surface conductivity for π -conjugated organic semiconducting materials. So, controlling the chemical species of the insulator surface and/or tailoring the surface energy are the most popular methods for altering the characteristics of a semiconductor/insulator interface to improve the V_{th} , carrier mobility and ON/OFF ratio of the device. Note that the magnitude of the effect depends upon the chemical structure of alkyl tail of SAMs [9, 10]. In addition, it is generally believed that the density and order of the SAM strongly affect the semiconductor nucleation mechanism and grain size. The nucleation has been identified as the most important stage of film growth for controlling the bulk film morphology and is highly dependent on the chemical and topological composition of the substrate [11–13]. The growth studies of organic thin film experimentally and theoretically have proven that the grain size and density of grain boundaries directly affect the field-effect mobility.

In addition, the long-term environmental stability of OFETs is a critical issue that must be addressed before its commercialization. For example, the display devices need a very long operating time. The gate-bias stress instability leads to a decrease in current and shift of the V_{th} (and correspondingly drain-source current changes), under a constant applied bias. As a consequence of the instability, the brightness of OLED, OLFET and liquid crystal display (LCD) driven by an OFET will vary inhomogeneously with time, because the ON-current varies with stress time in the presence of a prolonged gate bias. Furthermore, the device might not turn ON/OFF appropriately when the V_{th} shift exceeds the operating voltage of the devices [14]. To overcome such problems, effective approaches are necessary.

Vacuum deposition of organic semiconductors attempts to lower the fabrication complexity related to the *in situ* chemical purification of materials by sublimation, low unintentional doping, lack of solvent use, and precise control of deposition conditions in terms of film quality (smoothness) and thickness. These devices are quite reproducible as compared to the solution processed OFET devices. In this regard, metal phthalocyanine derivatives and vacuum processed organic semiconductors have been researched for many years to understand the growth modes as a function of substrate composition and their resultant performance in field-effect transistors. The devices made with metal phthalocyanine molecules are usually stable, both thermally and chemically, and they are widely used for solar cells, optical limiters, and photoconductors [15]. It is worth pointing out that some of the original high mobility organic semiconductors that are cited throughout as constant references, such as pentacene and Poly(3-hexylthiophene) (P3HT), suffer from chemical instabilities when exposed to ambient conditions during gate bias stress [16–18].

Under vacuum conditions, the performance of VOPc based OFET has been reported to be good using very thin (~ 3 nm) ordered para-hexaphenyl (p-6P) layer as a substrate modification and SiN_x as the gate dielectric layers [19–21]. However, this requires extra steps to fabricate the device and leads to cost escalation. It may be noted that p-6P is a very costly material (~ 400 \$ for 250 mg, Alfa Aesar) and is patented by Garnier *et al*, which hinders low cost fabrication of optoelectronic devices. Furthermore, in these devices the time constant is extracted from the shift of V_{th} in transfer curves (as a function of bias stress time) after giving relaxation to the devices during each scan. It has several drawbacks, as it is a slow process (at the very initial time, the information is not available) and the extracted V_{th} is complicated, due to fact that most of the OFETs do not show a linear regime (at extra plotted transfer curves (I_{DS})^{1/2} versus V_{GS}) even though transfer curves shift clearly [22]. Here, we have used a more efficient approach to extract the time constant. Instead of measuring a full transfer curve, the drain current (I_{DS}) is measured as function of the prolonged bias stress time at a constant applied gate-source voltage (V_{GS}) and a source-drain voltage (V_{DS}).

In this work, we have studied the performance of VOPc based OFETs under ambient conditions with a hexamethyldisilazane (HMDS) treated SiO₂ layer and a bare/non-treated SiO₂ layer. To the best of our knowledge, there is no report on HMDS treated VOPc based high performance OFETs under ambient conditions, which is important for the low-cost fabrication of practical devices. We also present the influence of the chemical species on the insulator surface on the shift in V_{th} that is induced by the gate bias stress in top contact transistors with VOPc as an active layer. We attempt to trace the microscopic origin of the superior performance of the HMDS treated device, as compared to that of the non-treated substrate. It is shown that a strong bias stress instability found for non-treated SiO₂ layer is likely to be caused by the inter-grain voids present in the active channel, besides the contribution from silanol group (Si-OH) at the dielectric interface as reported by most of the literature. In the case of the HMDS treated surface, the devices exhibited very low bias stress and low V_{th} shift. The bias stress stability data obey the stretched exponential decay with a characteristic time constant (τ) more than 20 times higher than that of the untreated SiO₂ case.

2. Experimental details

2.1. Substrate preparation and molecule stability

A highly p-doped silicon wafer covered with a 200 nm SiO₂ layer served as a common gate dielectric. Prior to the device fabrication, the substrates were cleaned thoroughly in deionized water, acetone and finally in 2-propanol, 15 min each by ultrasonication and subsequently dried using a N₂ gas blower. Next, the surface of the SiO₂ was exposed to a HMDS SAMs (short-chain length, high purity, and stable against moisture) (Alfa Aesar, 97%) vapor, which was heated at 120 °C for 1 h in order to reduce the surface energy and it served as a buffer layer (about 2 nm).

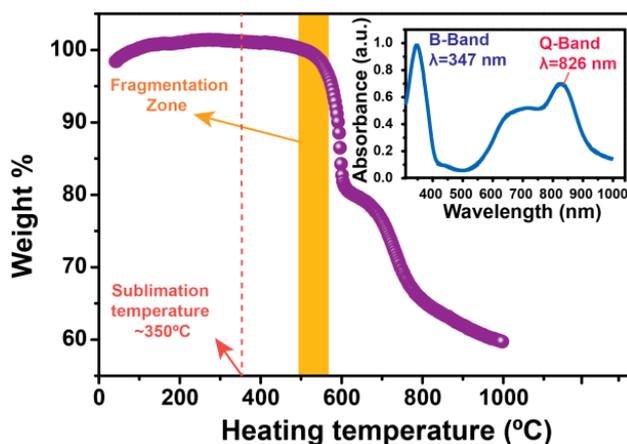


Figure 1. TGA plot for VOPc molecule (heating rate: $10\text{ }^{\circ}\text{C min}^{-1}$ with Ar gas). The inset shows the UV-vis absorption spectrum of 60 nm thick VOPc thin film grown at a substrate temperature $120\text{ }^{\circ}\text{C}$.

Thermogravimetric analysis (TGA) (NETZSCH) was carried out in Ar gas up to $1000\text{ }^{\circ}\text{C}$ at a heating rate of $10\text{ }^{\circ}\text{C min}^{-1}$ and it shows that the vanadium (IV) oxide phthalocyanine ($\text{C}_{32}\text{H}_{16}\text{N}_8\text{O}_V$) (acronym: VOPc) molecules (Alfa Aesar, 97%) are stable up to a temperature of $\sim 450\text{ }^{\circ}\text{C}$ (figure 1). Vapour deposition of organic molecule gives rise to better crystalline quality and a smoother surface as compared to the spin coating or solution immersion process.

2.2. Device fabrication and characterization

The VOPc organic molecules were sublimed at $\sim 350\text{ }^{\circ}\text{C}$ to deposit thin-films of thickness $\sim 60\text{ nm}$ on various substrates using an effusion cell based thermal evaporator (BESTEC, Germany) at a chamber pressure of $\sim 10^{-7}$ mbar with a growth rate of $\sim 0.4\text{ \AA s}^{-1}$. The thickness of the film was measured using a digital thickness monitor. In this case, as the sublimation temperature of VOPc molecules is $\sim 350\text{ }^{\circ}\text{C}$, based on the TGA result, we believe that the molecules are not fragmented during the deposition on various substrates. This is further confirmed from the UV-vis absorption spectrum of the VOPc film (see inset of figure 1), which shows features similar to other phthalocyanine molecules. The substrate temperature was kept constant at $120\text{ }^{\circ}\text{C}$ (lower than the fragmentation temperature of HMDS) to improve the device performance. Finally, to complete the device structure, a high work function ($\sim 5.1\text{ eV}$) Au metal of $\sim 60\text{ nm}$ thickness, which acts as source/drain electrodes with an Ohmic contact, was deposited through a stainless steel shadow mask, on the top of the VOPc film (HOMO level $\sim 5.5\text{ eV}$) by thermal evaporation at a vacuum level of 2×10^{-6} mbar. Contact electrodes were defined in a top-contact device configuration (see figure 2(a)) with a channel width (W) and length (L) of $2050\text{ }\mu\text{m}$ and $45\text{ }\mu\text{m}$, respectively. Figures 2(b) and (c) shows the cross-sectional field-emission microscopy (FESEM) image of HMDS treated and non-treated VOPc layer on the SiO_2 substrate. The surface morphology of the deposited VOPc thin film was examined by atomic force microscopy (AFM) in the tapping mode

with an Agilent-5500 AFM in ambient conditions. An x-ray diffraction (XRD) (Rigaku) pattern was measured with a $\text{Cu-K}\alpha$ source ($\lambda = 1.54056\text{ \AA}$). Before applying bias stress to the devices, at first all of the transfer and output curves were measured by a source-measure unit (Keithley, 2602A) in air ambient. After the reference measurement, the OFETs were stressed in the enhancement mode at constant V_{DS} and V_{GS} voltages under ambient conditions. V_{th} and charge carrier mobility (μ) were extracted from the transfer characteristic in the saturation region of the I_{DS} on the basis of the relation,

$$I_{\text{DS}} = \frac{\mu W C_i}{2L} (V_{\text{GS}} - V_{\text{th}})^2 \quad (1)$$

where V_{GS} is the gate-source voltage, L is the channel length, W is the channel width, and C_i is the dielectric capacitance per unit area.

3. Results and discussion

3.1. Morphology and structural characterization of VOPc thin films: non-treated and HMDS-treated substrates

In order to study the surface morphology, the VOPc-films were characterized by AFM in the tapping mode to avoid any damage to the soft film. Figure 3 shows the AFM images for two 60 nm thick films of VOPc grown at $120\text{ }^{\circ}\text{C}$. The images were recorded over an area of $2\text{ }\mu\text{m} \times 2\text{ }\mu\text{m}$ for both HMDS-treated and non-treated cases, respectively, as shown in figures 3(a) and (b) and the corresponding magnified views are shown in figures 3(c) and (d).

To calculate different statistical parameters of the grains in the film, such as grain volume, grain area and rms roughness, we also have acquired AFM images over $5\text{ }\mu\text{m} \times 5\text{ }\mu\text{m}$ area. The morphology for the VOPc film deposited on bare SiO_2 and HMDS treated SiO_2 is quite similar with a uniform granular structure. Almost void-free morphology can clearly be observed in the films on the HMDS-passivated SiO_2 substrate, as shown in figure 3(a). In contrast, it is evident that more voids in between the grains are present on the VOPc film shown in figure 3(b) with a circularly marked boundary for the non-treated SiO_2 substrate (arrows indicate voids location). Using Gwyddion software (watershed programme), the calculated grain sizes are $\sim 17.9\text{ nm}$ and $\sim 18.3\text{ nm}$ for the thin films on HMDS-treated SiO_2 and bare SiO_2 substrates, respectively. Note that the rms roughness (R_q) of the film is 7.49 nm in the HMDS treated case, which is slightly lower than the bare SiO_2 case (7.64 nm), due to lower surface energy. We calculated the rms roughness of the thin films to correlate it with the quality of films grown on different substrates. In general, a lower rms roughness implies a lower surface energy and better crystallinity of the films.

In order to investigate the crystalline quality of the VOPc films, we carried out XRD studies. The XRD pattern of the VOPc thin film with a thickness of 60 nm grown on HMDS-treated and non-treated case is shown in figure 4. The VOPc layer shows a distinct XRD peak at $2\theta \approx 7.5^{\circ}$ corresponding to the crystalline (010) planes of VOPc with

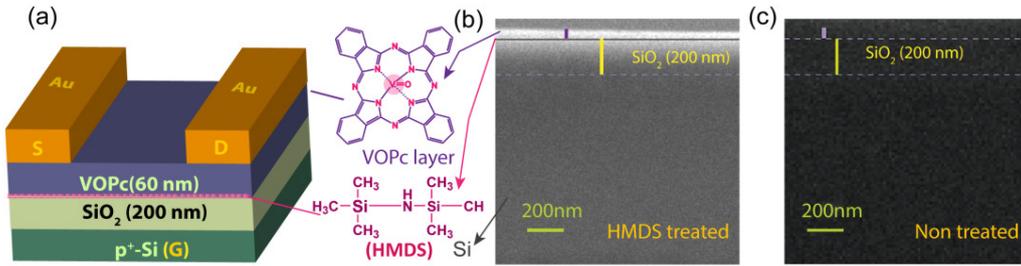


Figure 2. (a) Schematic of cross-section of bottom gate top contact VOPc based OFET along with the molecular structure of VOPc and HMDS. Cross sectional FESEM images of the VOPc film on (b) HMDS treated SiO₂, and (c) non-treated SiO₂ substrates.

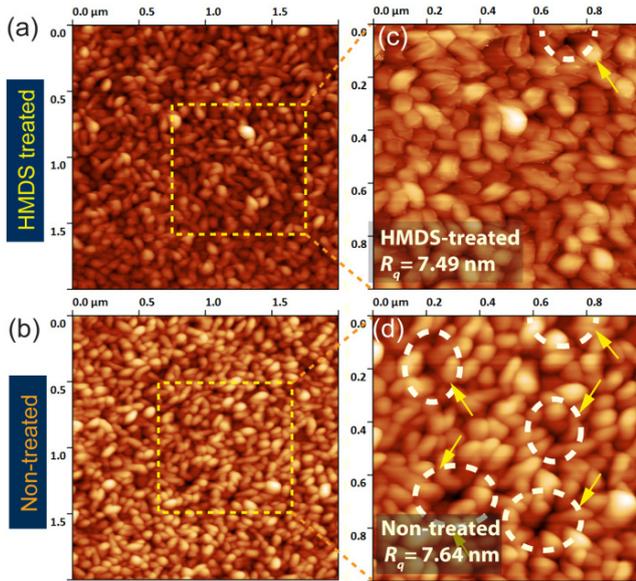


Figure 3. Tapping mode AFM images ($2 \mu\text{m} \times 2 \mu\text{m}$) of ~ 60 nm-thick VOPc thin film grown on (a) HMDS treated SiO₂, and (b) untreated SiO₂ layers. (c), (d) The magnified views ($1 \mu\text{m} \times 1 \mu\text{m}$) of images in (a) and (b), respectively. Dotted circular regions refer to the voids in-between the inter-grain regions in the VOPc layer. The RMS roughness, R_q of the surfaces is indicated in each case.

inter planar spacing $\approx 11.77 \text{ \AA}$ (phase II, triclinic, spacegroup $P\bar{1}$, $a = 12.027 \text{ \AA}$, $b = 12.571 \text{ \AA}$, $c = 8.690 \text{ \AA}$, $\alpha = 96.04^\circ$, $\beta = 94.80^\circ$, and $\gamma = 68.20^\circ$) thin films [23, 24]. We noticed that the intensity of the first order diffraction peak is significantly higher (by about 2.5 times) for the film on the HMDS treated substrate as compared to that on the bare SiO₂ substrate. However, no measurable shift in peak position is observed, indicating no change in the inter planar spacing in the two cases. It is worth noting that the XRD pattern provides information on the intermolecular ordering perpendicular to the substrate. Our result reveals that the ordering of VOPc molecules is highly improved with HMDS treatment and it can be hypothesized that the VOPc-molecules are arranged vertically on the HMDS treated substrate with lower surface energy than the case of bare SiO₂. The presence of distinct peaks in the XRD pattern of the VOPc film implies the formation of ordered crystalline film and intermolecular π - π stacking direction (herring-bone pattern) parallel to the substrate. This feature implies that the crystalline quality of the thin film is appropriate to expect the efficient transport of charge carriers in the OFET geometry.

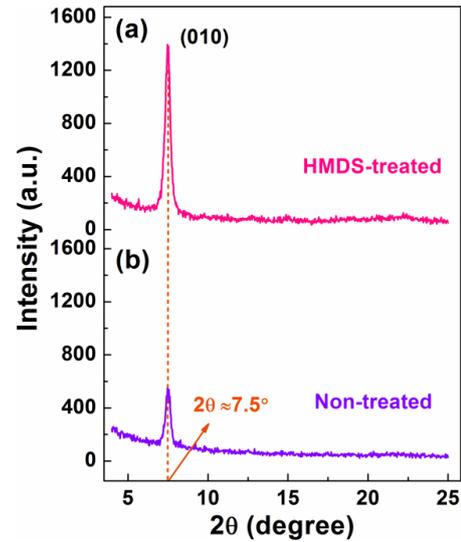


Figure 4. XRD pattern of 60 nm thick VOPc thin film on the SiO₂ substrate deposited at a substrate-temperature of 120 °C for (a) HMDS-treated and (b) non-treated case.

3.2. Electrical characterization of OFETs with HMDS treated and non-treated substrates

A schematic of the device structure of the bottom gate top contact OFET based on VOPc along with the chemical structure of VOPc and HMDS is shown in figure 2(a). Here, the VOPc layer acts as a p-channel and the hydrophobic HMDS thin buffer layer (~ 2 nm) serves as a surface modification agent for the SiO₂ dielectric. A series of bottom gate top contact devices were fabricated by using SiO₂ and HMDS-modified SiO₂ substrates for comparison. HMDS treated devices exhibit very good p-type field-effect characteristics. Figures 5(a) and (b) show the typical transfer ($I_{DS} - V_{GS}$, at $V_{DS} = -40$ V) and output characteristics ($I_{DS} - V_{DS}$, at $V_{GS} = 0, -10, \dots, -40$ V) curves of HMDS-treated, respectively. Similarly, figures 5(c) and (d) show the transfer and output characteristics of non-treated devices. For the HMDS-treated devices, the drain-source saturation current (I_{DS}) exhibits one order of magnitude higher current than the non-treated (bare) SiO₂ devices. The output curves show excellent linearity (Ohmic) in the region with low V_{DS} , demonstrating good Ohmic contact between the Au and VOPc layer. The saturation mobility and V_{th} are extracted from the linear fit to the square-root of I_{DS} versus V_{GS} curves for $V_{DS} = -40$ V. The transfer characteristic of I_{DS} versus V_{GS} for $V_{DS} = -40$ V exhibits a one order of magnitude

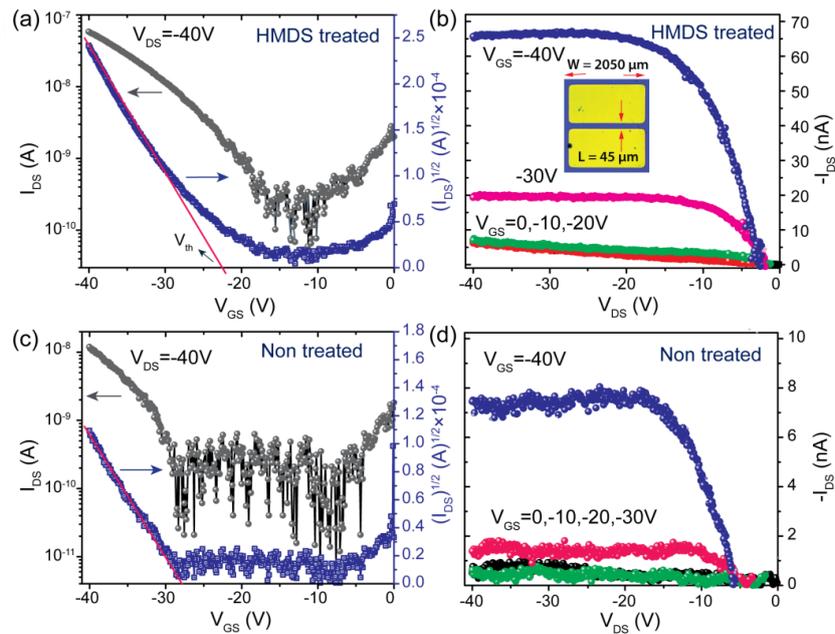


Figure 5. (a), (c) Transfer ($I_{DS} - V_{GS}$, $(I_{DS})^{1/2} - V_{GS}$) and (b), (d) output characteristics ($I_{DS} - V_{DS}$) for HMDS treated and non-treated SiO_2 substrates, respectively. The inset shows the fabricated VOPc OFET channel length (L) and width (W).

increase in the ON/OFF current ratio for the HMDS treated OFETs as compared to the devices with untreated devices.

3.3. Effect of surface modification on various OFET device parameters

It is also apparent that the devices based on the HMDS treated substrate exhibited much improved field-effect characteristics (figure 5(b)) than those devices on bare SiO_2 substrates (figure 5(d)). For example, the mobility of the devices on bare SiO_2 is calculated as $0.23 \times 10^{-3} \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ and the ON/OFF ratio is 10^1 – 10^2 , while the devices on HMDS-modified SiO_2 substrates exhibited a mobility of $\sim 0.1 \times 10^{-1} \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ and an ON/OFF ratio of 10^3 . Thus, the mobility of the devices on HMDS-modified SiO_2 substrates is nearly two orders of magnitude higher than that of the devices on non-treated SiO_2 . Note that the extracted mobility of the VOPc layer is relatively low as compared to some of the reported values (see e.g. $\mu_{th,avr} = 1.0 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, $V_{GS}, V_{DS} = 100 \text{ V}$ on the OTS modified substrate, $0.02 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, $V_{GS}, V_{DS} = 50 \text{ V}$ on the para-sexiphenyl (p-6P) monolayer) due to measurement at a relatively lower effective gate voltage and low crystallinity in VOPc thin films [19, 21, 25]. In the case of the bare SiO_2 layer, the surface contains a large number of polar silanol (Si-OH) groups, due to the air humidity and water (depending upon processing history), that act as a trap centre and result in the SiO_2 substrate being hydrophilic in nature. In contrast, the HMDS monolayer chemically bonds with the Si atom to the oxygen of oxidized surfaces, by the releasing of ammonia (NH_3). Here, $\text{Si}(\text{CH}_3)_3$ groups are responsible for the hydrophobic surface. The methyl groups of the HMDS fragment forms a hydrophobic surface and thus improves the resist wetting and adhesion. This whole process, how the hydrophilic surface turns into a hydrophobic surface, is schematically shown in figure 6.

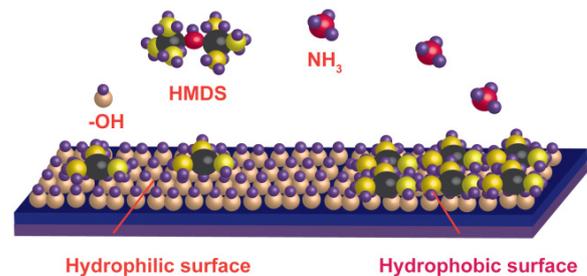


Figure 6. Schematic illustration of the mechanism of HMDS monolayer self-assembly on SiO_2 -oxidized surface and converting the hydrophilic surface into hydrophobic.

It should also be noted that the alkali ions in the SiO_2 layer also influence the device performance, particularly in hysteresis and V_{th} shift [26]. Previous reports suggest that the OFF-current can be significantly suppressed, due to reduced trap states and improved device performance [27].

It is commonly acknowledged that the structure (crystal phase composition, molecular ordering, and molecular orientation) and morphology (grain, boundary, and interconnection) of a semiconductor film play important roles on the carrier mobility in an organic thin film transistor. Therefore, characterization of the structure and morphology of VOPc film prior to device fabrication is necessary to understand the mechanism behind the improvement in performance after HMDS treatment. One of the possible explanations that emerges from the AFM analysis of figure 3 is that several inhomogeneous voids or charge trapping centers (indicated by the circular boundaries with arrows) are created on the film on the bare SiO_2 substrate, which is consistent with other reports [28], despite the fact that the surface grain features are almost identical in both cases. The flow of charges through the VOPc film is schematically shown in figure 7 for HMDS and non-treated substrates, respectively.

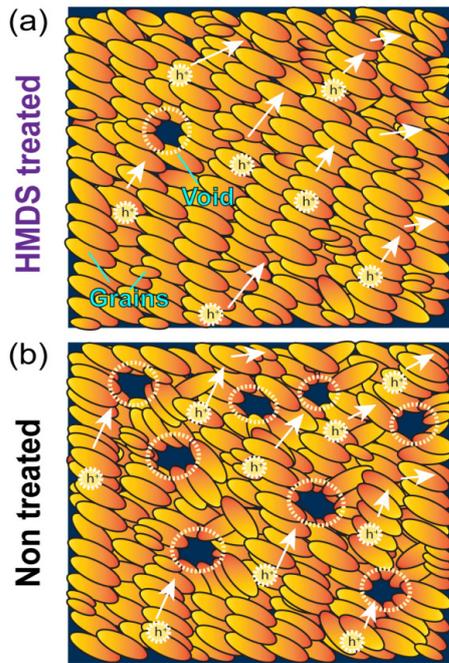
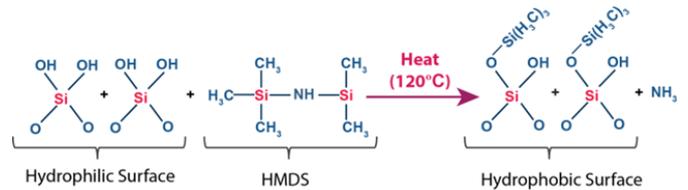


Figure 7. Schematic of VOPc films; the arrow heads show the direction of charge flow due to a voltage difference in case of (a) HMDS treated VOPc layers (very few voids are noticeable) and (b) non-treated (a large number of voids in between the grains or poorly connected grains, as indicated by dotted circular zones), respectively.

Based on the report by Kalb *et al* [29], the structural defects associated with grain boundaries are the primary cause of ‘fast’ hole traps in OFETs made with vacuum-evaporated pentacene. The major improvement in the device characteristics with the HMDS treatment may be attributed to the following factors. Firstly, a high density of HMDS may be covalently attached with the inorganic dielectric and cross-linking with the organic semiconductor. It optimizes the surface energy of SiO₂, which increases the adhesion of the organic semiconductor on the substrate and improves the π - π stacking structures in the herringbone of the VOPc film. Thus, the mobility is also improved as π - π stacking structures control the strong intermolecular interaction that enhances the stacking. From the AFM images of VOPc films shown in figure 3, a large number of closed grains and smooth surfaces can be observed. One explanation for the apparent disparity between grain size and mobility is due to the creation of voids in between the disconnected grains in 2D growth on a high energy surface, reducing the effective channel width of the transistor, and the voids are efficiently filled when 3D growth is favoured on a low energy surface [12, 13, 30]. So, the improved OFET device performance in the HMDS treated case is most likely due to the interconnectivity of VOPc grains at the semiconductor dielectric interface. The correlation between morphology (grain size/degree of crystallinity) and mobility is a key point that has been studied extensively, though unfortunately the exact relationship between the two remains unclear. Secondly, HMDS behaves as a silent coupling reactant, and the chemical reaction changes OH-terminated SiO₂ to a (CH₃)₃-Si surface [27]. Thus, the introduction of HMDS reduces the water molecules and OH-groups, and at the

same time the HMDS hydrophobic surface also makes it less dipolar, which improves the electrical properties. In essence, it provides an excellent interface with low traps and passivates the dangling bonds, which improves the charge transportation. The adhesion promoter HMDS makes the SiO₂ substrate hydrophilic to hydrophobic by the following reaction.



However, negative results are also reported for the passivation by using the other SAMs [31]. Thus, optimization of the growth and processing parameters may be the key to the improved device performance. However, the ongoing debate regarding the improved performance of devices with the insertion of the SAM layer may continue to exist.

3.4. Bias stress stability in OFETs and threshold voltage shift

After the standard DC characterization, the electrical response of VOPc based devices, both for bare and HMDS treated cases, has been investigated with respect to the bias stress effect. The bias stress phenomenon is analyzed by monitoring the time decay of I_{DS} upon static voltage polarization (fixed V_{DS} and V_{GS}). The bias stress effect has been investigated by recording the I_{DS} as a function of stress time under an applied gate bias V_{GS} of -40 V. The drain-source voltage (V_{DS}) has been fixed at -40 V for VOPc. Due to a prolonged bias stress in OFET, charge carriers trapped at the surface and/or interface result in the decay of drain current. The rate equation for the change of the free carrier density (N_{fr}) in OFETs accumulation channel can be given by $\frac{d}{dt}N_{fr} = -AD(t)N_{fr}$, where t is time, A is the proportionality constant related to the capture cross-section for mobile charge carriers, $D(t) = D_0 (\omega t)^\beta$ (where ω is the attempt-to-escape frequency, $\beta = T/T_0$ is the stretching parameter related to the barrier energy (height) for charge trapping ($0 < \beta \leq 1$)), a time dependent diffusion coefficient and this power law can apply universally, virtually for all the disorder systems which exhibit a dispersive transport [32–34] (see supporting information (stacks.iop.org/JPhysD/51/015110/mmedia) for a detailed derivation). Now for the threshold voltage shift ($\Delta V_{th}(t)$), one can customarily write that an OFET at stress time t is basically related to the trapped charges and can be given by $\Delta V_{th}(t) = \frac{eN_{tr}(t)}{C_i}$, where e is the charge, C_i is the capacitance of the gate dielectric, and $N_{tr}(t) = N_{tr}(0) - N_{fr}(t)$. Consequently, the shift in V_{th} (after applying the boundary condition) $\Delta V_{th}(t)$ is proportional to $\left[1 - \exp\left\{-\left(\frac{t}{\tau}\right)^\beta\right\}\right]$, i.e. $\Delta V_{th}(t) = [V_{GS} - V_{th}(0)] \times \left[1 - \exp\left\{-\left(\frac{t}{\tau}\right)^\beta\right\}\right]$, where τ is the relaxation time (see supporting information). Therefore, the decay of $I_{DS}(t)$ can be expressed after approximation as a stretched exponential function [35],

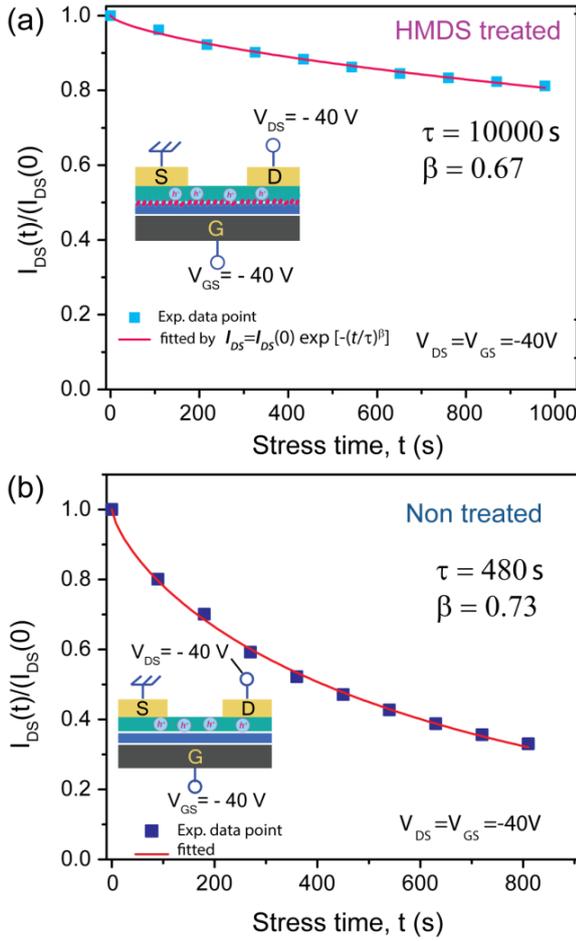


Figure 8. Normalized drain-source current $I_{DS}(t)/I_{DS}(0)$ as a function of bias-stress time (t) under ambient conditions for (a) HMDS treated SiO_2 , and (b) untreated SiO_2 layers.

$$I_{DS}(t) = I_{DS}(0) \exp \left[- \left(\frac{t}{\tau} \right)^\beta \right] \quad (2)$$

where $I_{DS}(0)$ is the initial maximum I_{DS} measured at the beginning of stressing. The experimental curves have been fitted with this stretched exponential decay function. Although the stretched exponential model was originally developed to describe the bias stress effect in amorphous silicon transistors considering the time-dependent evolution of trap states due to hydrogen migration [36], we employ the formalism here to describe a dispersive trapping process (which is widely used in virtually all the disordered systems) in p-channel OFETs. Interestingly, a stretched exponential function (equation (2)) provides a perfect fit to the data in both HMDS treated and non-treated systems.

Figures 8(a) and (b) show the data points (symbols) as well as fitted lines using equation (2). Fitting parameters τ and β are indicated in the figure in each case. The values of τ at room temperature extracted from the fitting are $\sim 10^4$ s and ~ 480 s in HMDS treated and non-treated devices, respectively. The corresponding exponent values are $\beta = 0.67$ and 0.73 , respectively. The large τ value in the HMDS treated case implies a long-term stability of the device, which is very much

desirable for practical applications. It should be pointed out that our results for HMDS treated systems is quite comparable to that of earlier reported p-type semiconductors, where the τ value on a tetracene based single crystal OFET was $\tau = 3.1 \times 10^4$ s, one order less compared to TIPS-pentacene systems ($\tau \sim 1.8 \times 10^5$ s) reported by Lee *et al* [37]. This analysis reveals that VOPc-OFETs based on a bare SiO_2 substrate are much more sensitive to the bias stress than the HMDS treated devices. Indeed, for the HMDS-treated devices, the current decreases by only $< 15\%$ after 900 s of constant bias (V_{GS}) application, while for the non-treated/bare devices the current reduction is as large as $> 70\%$. For the HMDS treated case, τ is about 20 times higher than the untreated device. Considering the improvement under ambient conditions, this is a significant achievement from the practical application point of view.

Note that the mechanism behind the trapping and poor performance of OFET devices is under debate. Sharma *et al* [38] proposed a proton migration mechanism involving water, while Lee *et al* [37] assumed direct drift/diffusion of holes into the dielectric. Long term charge trapping in devices with SiO_2 is known to be due to trapping in the SiO_2 layer reported by Mathijssen *et al* [39, 40]. There are various other possible sources of charge trapping inside OFET devices, like ionic conduction, degradation of contacts, charge trapping at the interface or in the bulk, diffusion of charges into the grain boundaries, etc [41]. One of the other possibilities that cannot be ignored is the Au top contact, which can create deep traps. In fact, some of the previous works have shown that carrier trapping in the long channel of the Au devices was indirectly caused by the deep trap states at the pentacene-dielectric interface in the contact region generated by Au penetration [42]. It is worth mentioning that we performed bias stress stability studies on SnCl_2Pc based OFETs using Ag and Al as source/drain contacts, which resulted (not shown) in characteristics time constants, $\tau \sim 10^5$ s (Ag) and 10^3 s (Al), respectively. So, it is clear that the contact electrode strongly influences the bias stress stability of the device.

The square-root of linear transfer characteristics at $V_{DS} = -40$ V as a function of bias stress time (before and after 15 min bias stress) under ambient conditions are shown in figures 9(a) and (b) for the HMDS treated and bare case, respectively. The relative V_{th} shifts ($|\Delta V_{th}|$) for HMDS-treated devices is much smaller ($\Delta V_{th} = 2$ V) than the devices with the bare SiO_2 layer ($\Delta V_{th} > 5$ V). If we assume that ΔV_{th} originated from trapped charges at the active layer-insulator interface, the density of interface-traps ($N_t \approx C_i |\Delta V_{th}| / q$, C_i is the capacitance per unit area of dielectric insulator and q is the elementary charge) [43] is calculated as $2.12 \times 10^{11} \text{ cm}^{-2}$ in HMDS treated-devices, which is much less than the bare case ($5.31 \times 10^{11} \text{ cm}^{-2}$). With stress time, the transfer curves shift in the direction of the applied gate bias to more negative voltages, as shown in figure 9. It clearly shows that the shift in V_{th} is smaller in the HMDS treated devices than that of untreated devices. The shift in V_{th} is indicative of the charge trapping instabilities in transistors. These results are very significant and it is believed that the water-related charge traps are reduced by passivation with HMDS on SiO_2 [34, 44].

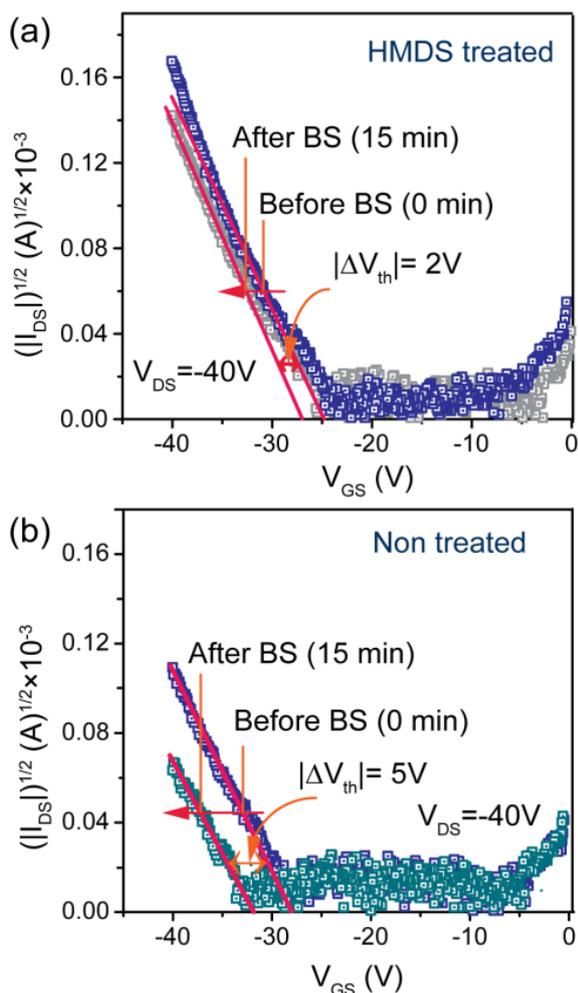


Figure 9. Threshold voltage shift (before and after 15 min bias stress) for: (a) HMDS-treated, and (b) untreated devices operated under ambient conditions.

The main effect of gate bias stress is a shift in the V_{th} , a typical case for organic transistors, which can thus be avoided by simple HMDS treatment.

4. Conclusions

HMDS passivation of a SiO_2 dielectric layer shows high performances and better air stability of VOPc OFETs than the devices with a non-treated SiO_2 layer. The devices with top contact Au electrodes exhibit excellent p-channel behavior with high hole mobility for HMDS-treated devices. A bias stress stability study under ambient conditions shows stretched exponential decay behavior during long term operation under constant bias voltage with the resulting decay of the drain current by only $\sim 15\%$ for the HMDS-treated case, while it shows a very sharp fall by $\sim 70\%$ for the devices with a bare SiO_2 layer. The corresponding characteristic time constant (τ) is calculated as 10^4 s for the HMDS-treated case, while it is very low (~ 480 s) for the bare/non-treated substrate case. The high bias stress stability of the HMDS treated VOPc based OFET was primarily attributed to the absence of voids and the efficient transport of charge carriers at the dielectric/semiconductor

interface, due to closely packed molecular grains of VOPc on the HMDS monolayer. Thus, HMDS treated devices with long term stability are very promising for practical applications. For low performance devices based on bare SiO_2 , it is believed that the charge trapping occurs primarily at the voids in the inter grain regions of the active semiconductor film, while it is almost negligible for the HMDS-treated SiO_2 case.

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